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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/491,302	01/25/2000	John D. Geissinger	55271USA6A	8370

32692 7590 03/15/2004

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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/491,302	GEISSINGER ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 8-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The Affidavit filed on September 19, 2002 under 37 CFR 1.131 has been considered but is ineffective to overcome the Fujisawa reference.

2. The evidence submitted is insufficient to establish a conception of the invention prior to the effective date of the Fujisawa reference. While conception is the mental part of the inventive act, it must be capable of proof, such as by demonstrative evidence or by a complete disclosure to another. Conception is more than a vague idea of how to solve a problem. The requisite means themselves and their interaction must also be comprehended. See *Mergenthaler v. Scudder*, 1897 C.D. 724, 81 O.G. 1417 (D.C. Cir. 1897). The evidence does not show the whole invention as claimed for at least the reason that an interconnect member connected between each of the conductive layers of the capacitor is not shown.

Claim Objections

3. It is noted that in the amendment filed January 23, 2004 that applicant has labeled claims 5 – 7 and 20 – 26 as "withdrawn". Applicant cancelled claims 5 – 7 and 20 – 26 in the amendment filed July 7, 2003, and therefore, these claims are cancelled for all further prosecution.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 – 4 and 8 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kling et al. (US 2002/0048927 A1, Kling) in view of Brandt et al. (USPAT 6068782, Brandt).

With regard to claim 1, Kling discloses in figure 1 an electronic package. Kling discloses in figures 1 – 3b a conductive trace layer (Pads in figure 3b) having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads. Kling discloses in figures 1 – 3b a dielectric substrate (16, see figure 1) mounted on the first side of the conductive trace layer. Kling discloses in figures 1 – 3b and paragraph 18 an embedded capacitor (14 in figure 1) having a capacitance of 50 nF/sq.cm including a first conductive layer (Power plane, figure 3b), a second conductive layer (Digital ground plane, figure 3b) and a layer of dielectric material (labeled AlO_2 in figure 3b) made of a non-conductive polymer (polyimide) disposed between the first and the second conductive layers, the first conductive layer attached to the second side of the conductive trace layer by a first adhesive layer (labeled SiO_2 in figure 3b). Kling does not disclose that the dielectric material is made of a non-conductive polymer blended with high dielectric particles. Brandt discloses in column 4, lines 18 – 41 a suitable dielectric material made of a non-conductive polymer blended with high dielectric particles. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the dielectric material of Brandt in the method of Kling in order to tune the electronic properties of a

capacitor component as stated by Brandt in column 4, lines 22 – 41. Further, Kling teaches in paragraph 18 that any suitable dielectric material. Kling discloses in figures 3a and 3b a plurality of interconnect regions (one shown in figure 3b just to the right of the "AlO_2" arrow) extending through the first conductive layer and the dielectric material layer of the capacitor. Kling discloses in figure 1 an interconnect member (in figure 3b shown as the dark line lining the interconnect regions) connected between each of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected to a first set of the interconnect pads and the second conductive layer on the capacitor being electrically connected to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions.

With regard to claim 2, Kling discloses in figures 1 – 3b wherein the first electrode is maintained at a first reference voltage and wherein the second electrode is maintained at a second reference voltage different from the first reference voltage. It is well known in the art that power and ground planes are maintained at reference voltages.

With regard to claim 3, Kling discloses in figure 1 and in paragraph 38 an electrically conductive stiffening member (12) attached to the second conductive layer of the capacitor by a second adhesive layer (dark line between capacitor and substrate).

With regard to claim 4, Kling discloses in figure 1 and paragraph 38 a device receiving region (directly under 22) extending through the dielectric substrate, the conductive trace layer and the capacitor, and further comprising an electronic device (22) attached to the device receiving region on the stiffening member by a third adhesive layer.

With regard to claims 8 – 9, Kling discloses in figure 1 a capacitor that has a capacitance of 50 nF/sq.cm. It is not clear if Kling teaches that the capacitor has a capacitance of about 2 nF/sq.cm. to about 30 nF/sq.cm. MPEP 2144.05 states that the optimization of ranges within the prior art conditions, or through routine experimentation is obvious. It would have been obvious to one of ordinary skill in the art to use a capacitor that has a capacitance of about 2 nF/sq.cm. to about 30 nF/sq.cm because the optimization of ranges would have been obvious through routine experimentation in Kling. Further, Kling states in paragraph 34 that one of ordinary skill in the art will be able to select a proper capacitance for the capacitor suitable to decouple the circuit.

With regard to claim 10, Kling teaches in figure 1 a capacitor that has a capacitance of 50 nF/sq.cm. It is not clear if Kling teaches that the capacitor has a capacitance of at least 30 nF/sq.cm. MPEP 2144.05 states that overlapping ranges are obvious. It would have been obvious to one of ordinary skill in the art to use a capacitor that has a capacitance of at least 30 nF/sq.cm in the device of Kling because the current claimed range and the disclosed range in Zhang[1] overlap. Further, Kling states in paragraph 34 that one of ordinary skill in the art will be able to select a proper capacitance for the capacitor suitable to decouple the circuit.

With regard to claim 11, Kling teaches in paragraphs 34 and 35 wherein the dielectric material thickness depends on the application. Brandt teaches in column 4, lines 35 – 37 wherein the dielectric material of a capacitor has a thickness of 10 um. It would have been further obvious to one of ordinary skill in the art at the time of the present invention to use the dielectric thickness of Brandt in the device of Kling in order to have a useful thickness for a dielectric layer of a capacitor in a semiconductor package as stated by Brandt in column 4, lines 35 – 37.

With regard to claim 12, Brandt discloses in column 4, lines 18 – 41 wherein the dielectric material of the capacitor includes a metal oxide.

With regard to claim 13, Brandt discloses in column 4, lines 18 – 41 the high dielectric constant particles are formed from a material of lead zirconium titanate.

With regard to claim 14, Kling discloses in figures 1 – 3a wherein the dielectric substrate (first layer of 16) includes a plurality of apertures, each one of the apertures being positioned adjacent to one of the interconnect region of the capacitor.

With regard to claims 15 – 16, Kling discloses in figures 1 – 3a and paragraph 32 wherein the dielectric substrate includes a polyimide. It should be noted that Kling directly references Eichelberger (USPAT 5841193) for this teaching in paragraph 32.

6. Claims 17 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kling and Brandt as applied to claim 1 above, and further in view of Fujisawa et al. (USPAT 6184567, Fujisawa).

With regard to claim 17, Kling discloses in figures 1 – 3 an interconnect member. Kling does not teach that the interconnect member is a solder plug. Fujisawa discloses in figure 1 wherein the interconnect member is a solder plug. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the solder plug of Fujisawa in the device of Kling and Brandt in order to electrically fill the interconnect with a material which is widely available and understood in the art.

With regard to claim 18, Kling discloses in figure 1 wherein an interconnect pad. Kling does not teach wherein each interconnect pad is a solder pad. Fujisawa teaches in figure 8 interconnect pad (28 and 32) is a solder pad. It would have been obvious to one of ordinary skill

in the art at the time of the present invention to use the solder pad of Fujisawa as the interconnect pad in the device of Kling and Brandt in order to use pad material which is widely available and understood in the art.

With regard to claim 19, Kling discloses in figure 1 wherein the dielectric substrate has an aperture (filled by filler) extending therethrough adjacent each interconnect pad. It would have been further obvious in the method of Kling, Brandt and Fujisawa that the dielectric substrate has an aperture extending therethrough adjacent each solder ball pad.

Response to Arguments

7. Applicant's arguments filed January 23, 2004 have been fully considered but they are not persuasive.

8. With regard to applicant's argument that: "Applicants respectfully submit that the Office Action misinterprets the teachings of Kling. The Office Action states that item 16 in Fig. 1 of Kling is a dielectric substrate. However, it is clearly stated in Kling that item 16 is an interconnect layer having at least one metal layer. See, e.g., paragraphs 27 and 40. Accordingly, Kling does not disclose a dielectric layer mounted on one side of a trace metal layer;" It should be noted that Kling discloses in paragraph 40 "interconnect layer 16 can be formed on top of the component layer. In one practice, and in situ process can be performed wherein a **dielectric layer** is directly deposited on the upper surface of the plurality of components, in this case the decoupling capacitors 14 and the resistive element 22. Further processing can include **patterning and forming vias in the in situ formed dielectric layer**." [emphasis added] It can

be seen from this quotation that interconnect layer 16 comprises at least one dielectric layer, and thus interconnect layer 16 can be considered a dielectric layer. There is no evidence on the record that suggests an interconnect layer comprising both dielectric layers and metal layers cannot be considered a dielectric layer. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

9. With regard to applicant's arguments that: "Additionally, the Office Action states that the SiO_2 (silicon oxide) layer in Fig. 3b is an adhesive. Applicants submit that it is known in the art that SiO_2 is not an adhesive. Furthermore, Kling does not teaches the use of an adhesive layer between a conductive trace layer and a conductive layer of a capacitor;" First, it should be noted that applicant does not provide any evidence that "it is known in the art that SiO_2 is not an adhesive." Nothing on the record suggests that SiO_2 is not an adhesive. Second, it should be noted that "SiO_2" is only referred to as a label "a first adhesive layer (labeled SiO_2 in figure 3b)." Paragraph 18 explicitly gives examples of other materials that are well-known adhesives (i.e. polyimide). In this case, a layer labeled SiO_2 is attaching the first conductive layer to the second side of the conductive trace layer. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-2723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1164. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II

Tom Thomas
Supervisory Patent Examiner
Technology Center 2800